Fig.1

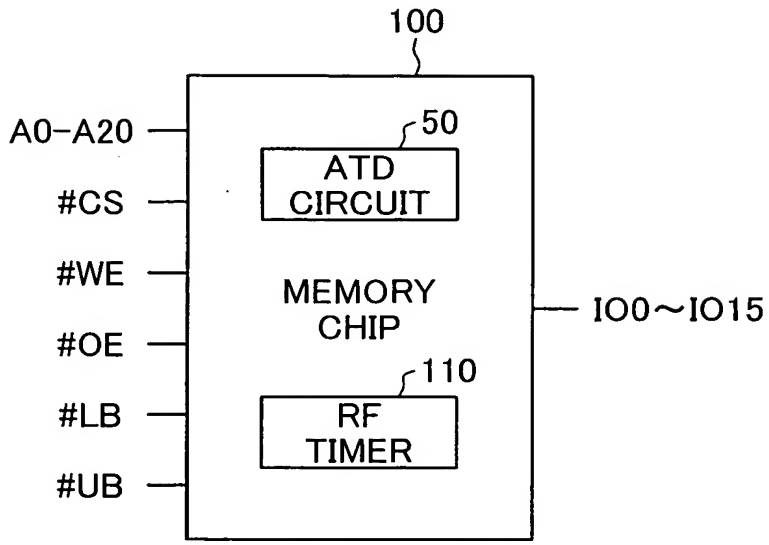


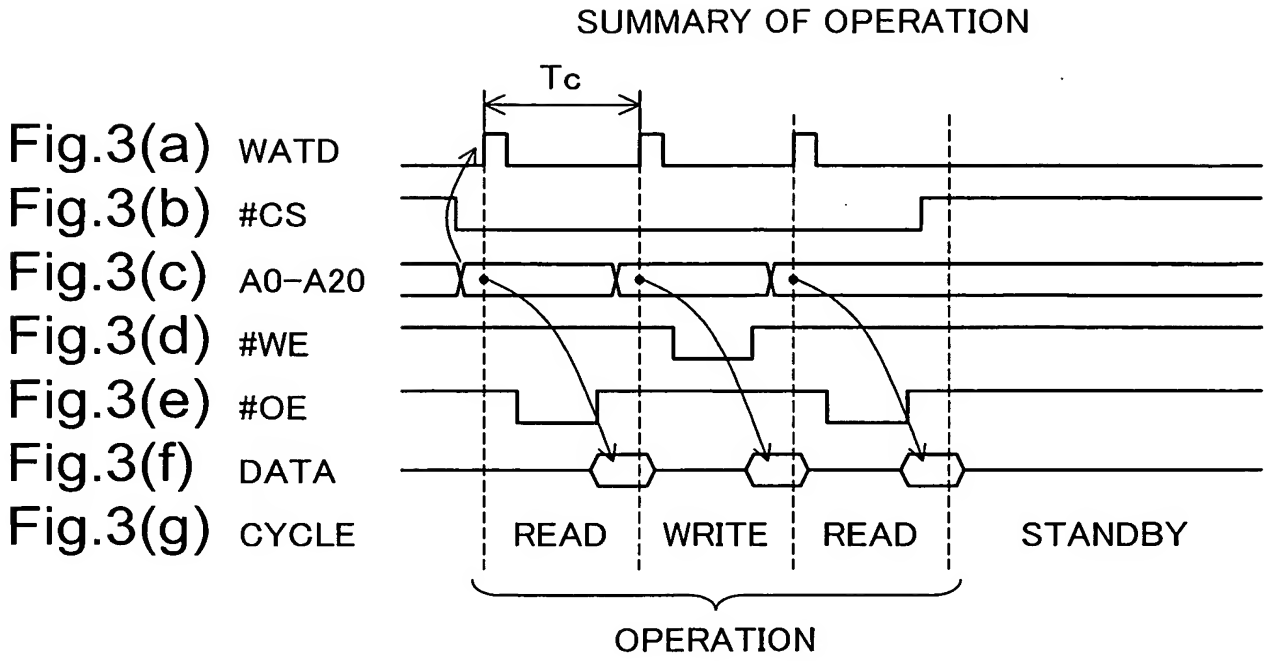
Fig.2

	#CS	REFRESH MODE (*)
OPERATION	L	MODE 1
STANDBY	H	MODE 2

(*)

REFRESH MODE 1 : REFRESH OPERATION IS EXECUTED SYNCHRONOUSLY WITH PATD SIGNAL AFTER REFRESH TIMING SIGNAL IS GENERATED IN MEMORY CHIP

REFRESH MODE 2 : REFRESH OPERATION IS EXECUTED IN RESPONSE TO GENERATION OF REFRESH TIMING SIGNAL IN MEMORY CHIP (ADDRESS INPUT UNNECESSARY)


SUMMARY OF OPERATION
Tc
Fig.3(a) WATD
Fig.3(b) #CS
Fig.3(c) A0-A20
Fig.3(d) #WE
Fig.3(e) #OE
Fig.3(f) DATA
Fig.3(g) CYCLE
READ
WRITE
READ
STANDBY
OPERATION

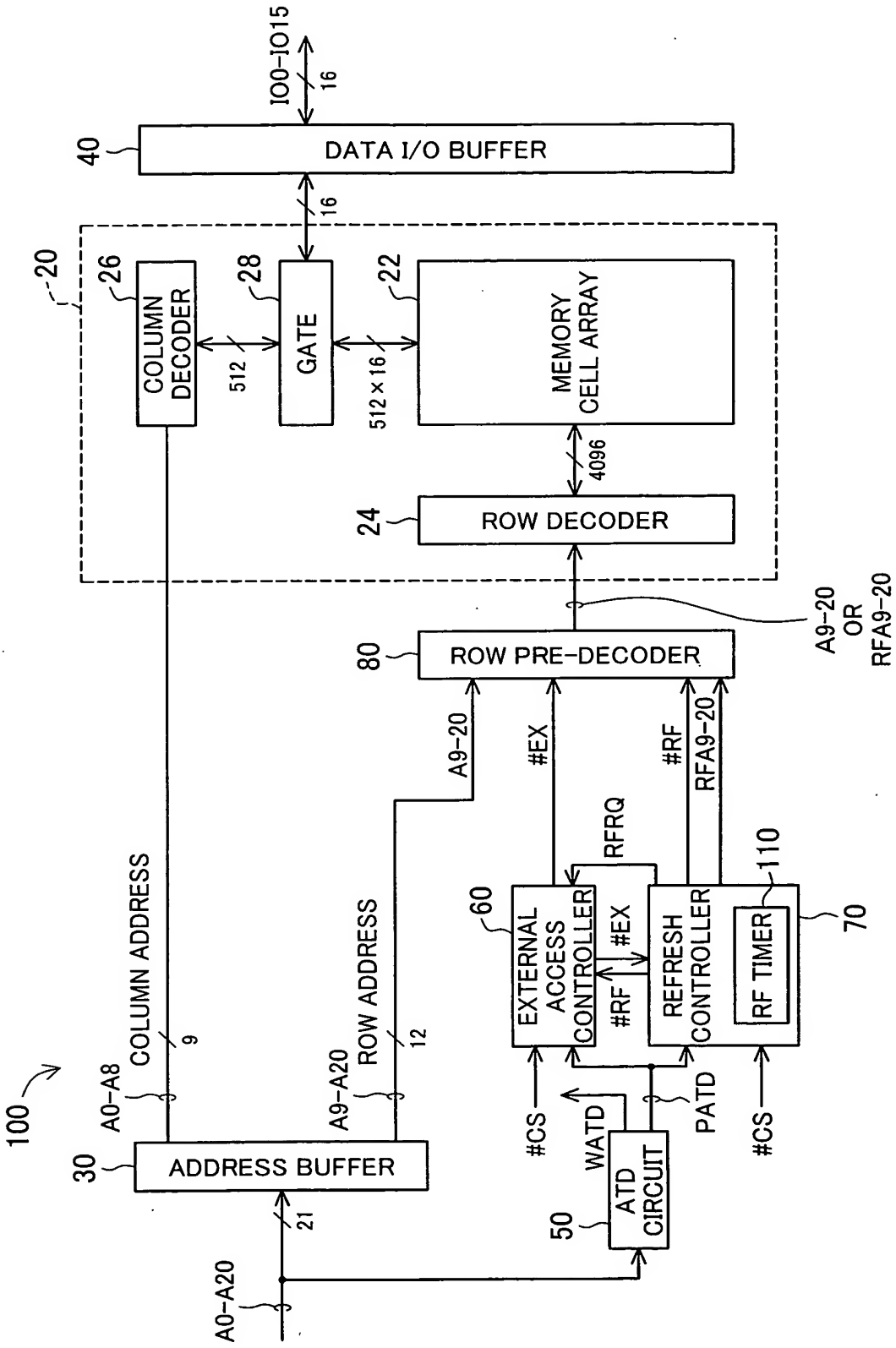

100
IO0-IO15
16
40
DATA I/O BUFFER
16
20
26
COLUMN DECODER
512
28
GATE
512 x 16
22
MEMORY CELL ARRAY
4096
24
ROW DECODER
A9-20 OR RFA9-20
80
ROW PRE-DECODER
A9-20
#EX
#RF
RFA9-20
RFRQ
110
60
EXTERNAL ACCESS CONTROLLER
#EX
#RF
REFRESH CONTROLLER
RF TIMER
70
COLUMN ADDRESS
9
ROW ADDRESS
12
A0-A8
A9-A20
#CS
WATD
PATD
#CS
30
ADDRESS BUFFER
21
50
ATD CIRCUIT
A0-A20

Fig.4

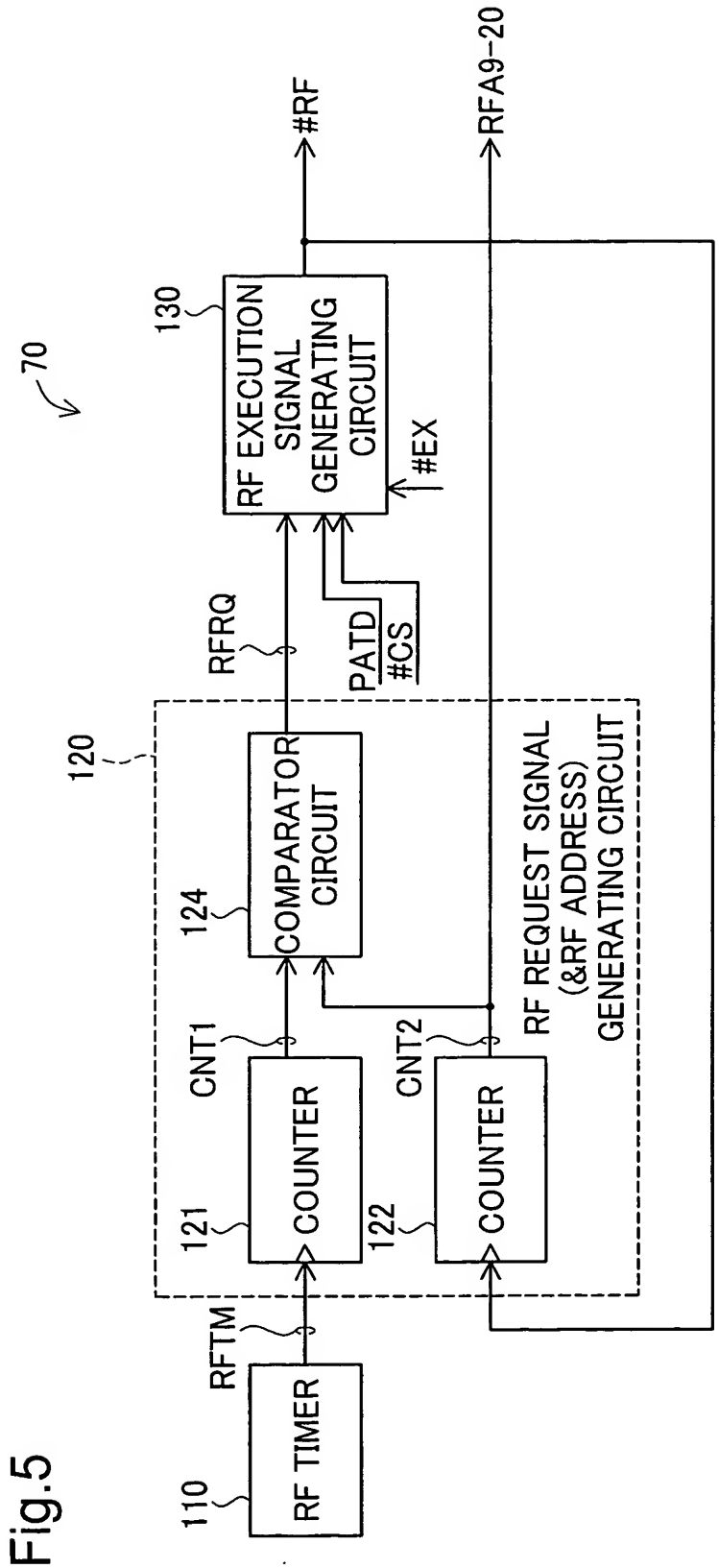

70
110
RF TIMER
RFTM
120
121
COUNTER
CNT1
122
COUNTER
CNT2
RF REQUEST SIGNAL
(&RF ADDRESS)
GENERATING CIRCUIT
124
COMPARATOR
CIRCUIT
RFRQ
PATD
#CS
130
RF EXECUTION
SIGNAL
GENERATING
CIRCUIT
#EX
#RF
RFA9-20

Fig.5

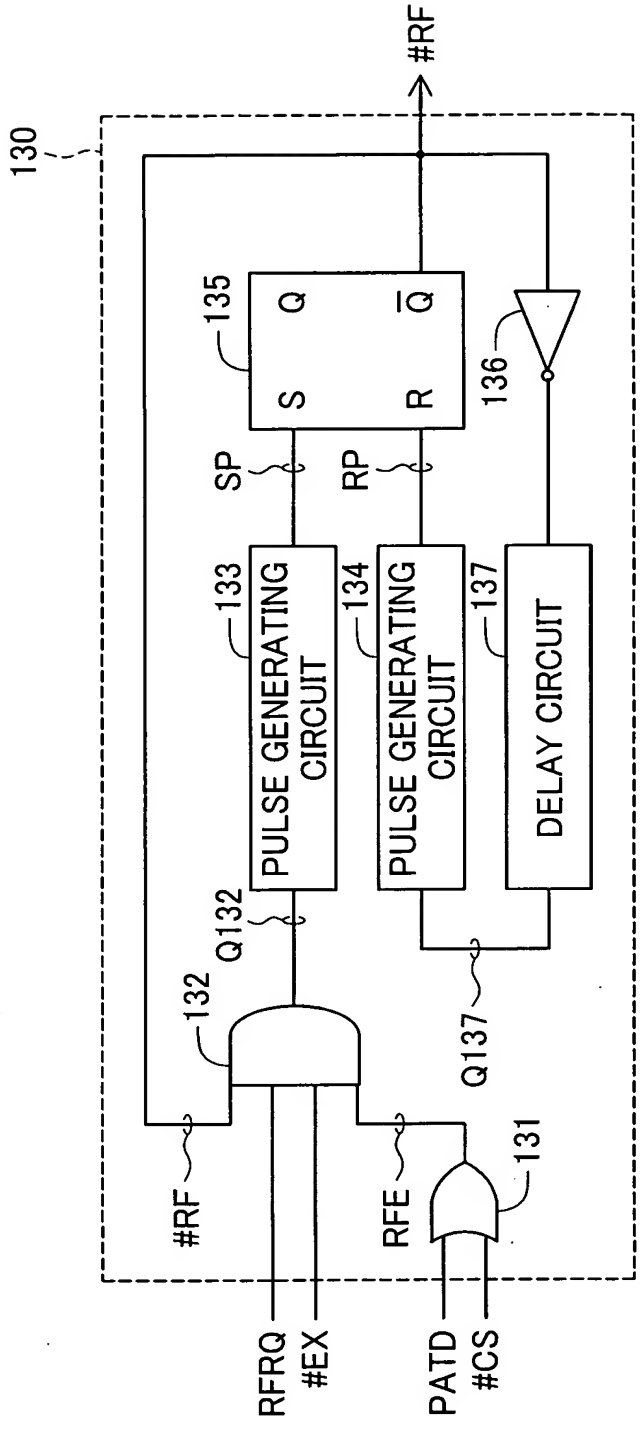

130
#RF
135
Q
$\overline{Q}$
S
R
136
SP
RP
133
PULSE GENERATING CIRCUIT
134
PULSE GENERATING CIRCUIT
137
DELAY CIRCUIT
Q132
132
Q137
#RF
RFE
131
RFRQ
#EX
PATD
#CS

Fig.6

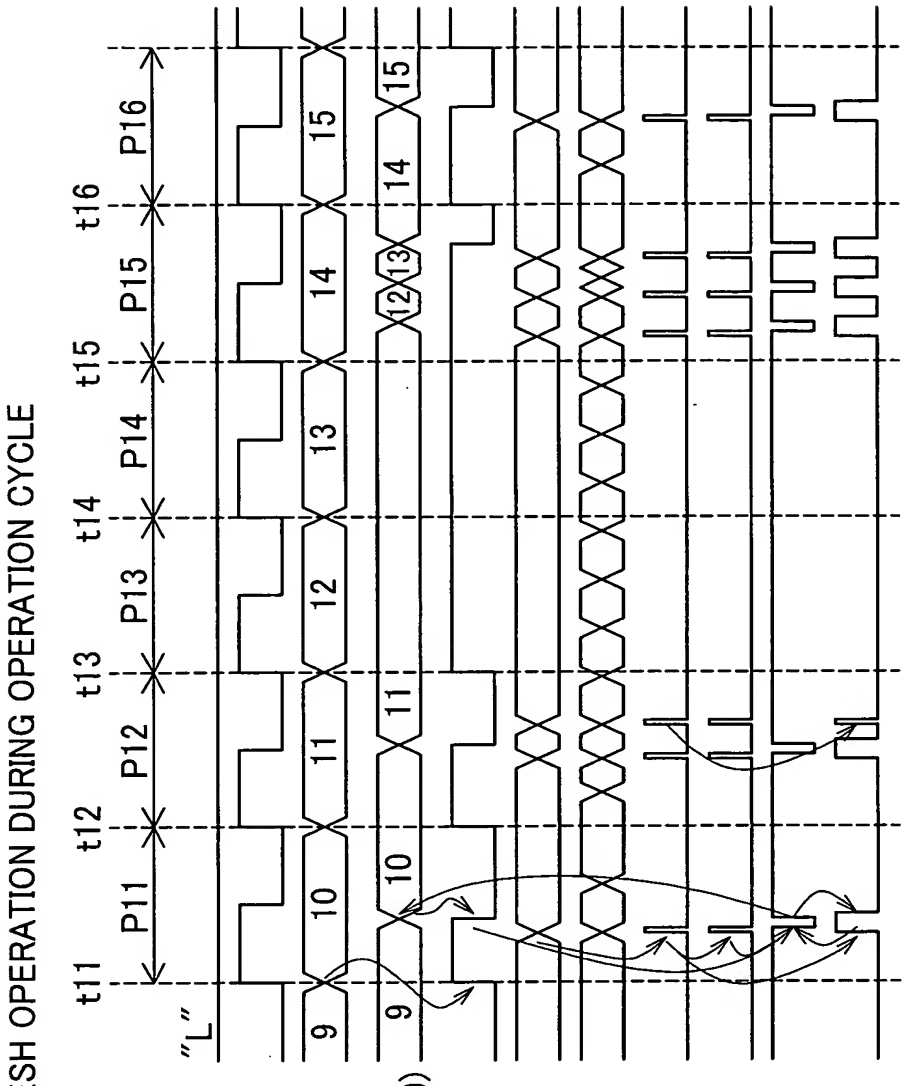


Fig.7(a)
Fig.7(b)
Fig.7(c)
Fig.7(d)
Fig.7(e)
Fig.7(f)
Fig.7(g)
Fig.7(h)
Fig.7(i)
Fig.7(j)
Fig.7(k)

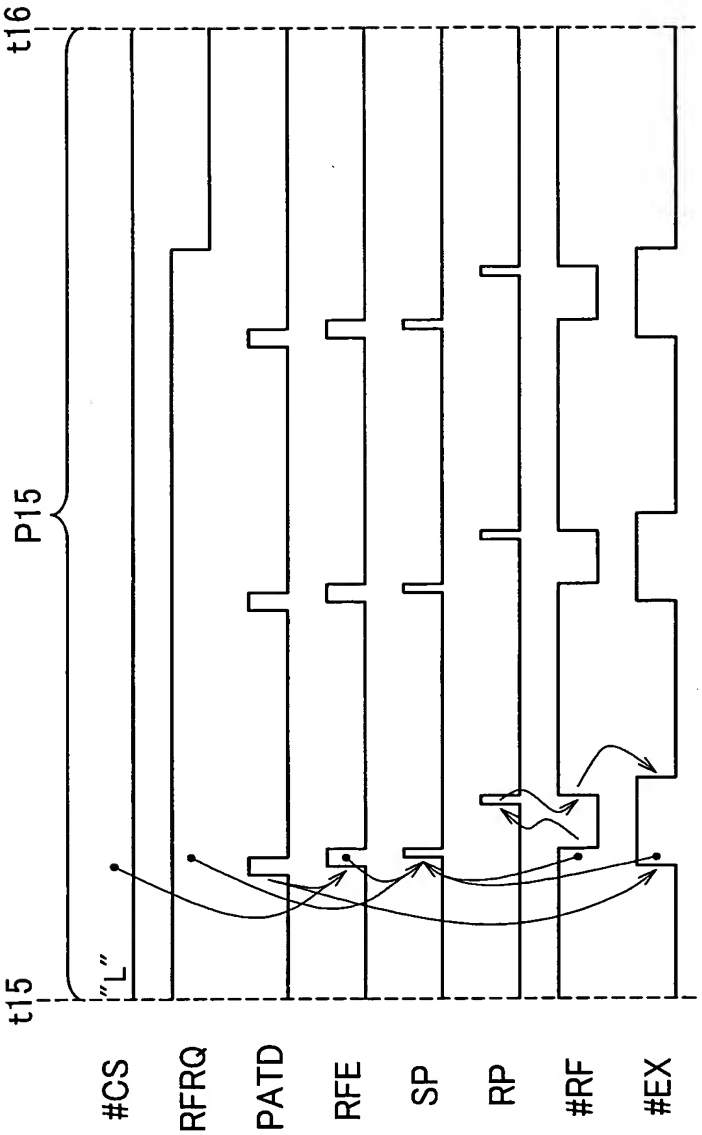


Fig.8

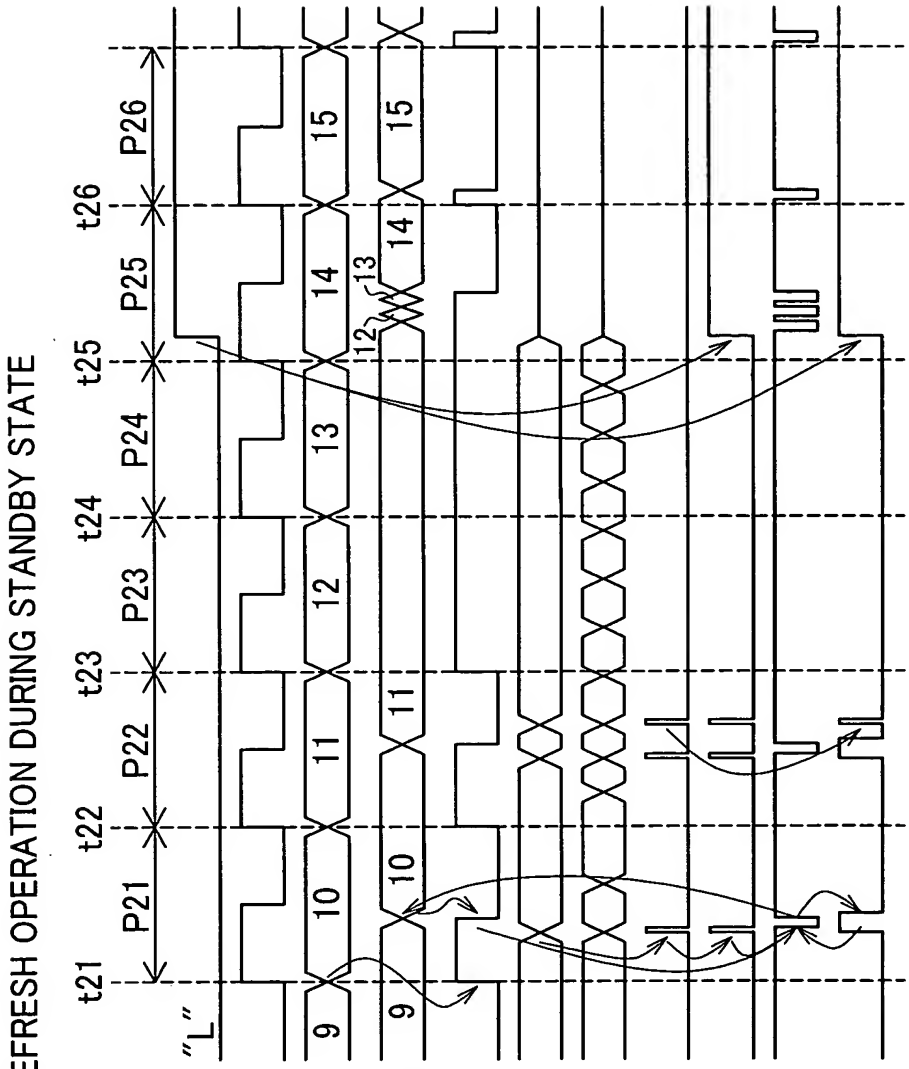


Fig.9(a)
Fig.9(b)
Fig.9(c)
Fig.9(d)
Fig.9(e)
Fig.9(f)
Fig.9(g)
Fig.9(h)
Fig.9(i)
Fig.9(j)
Fig.9(k)

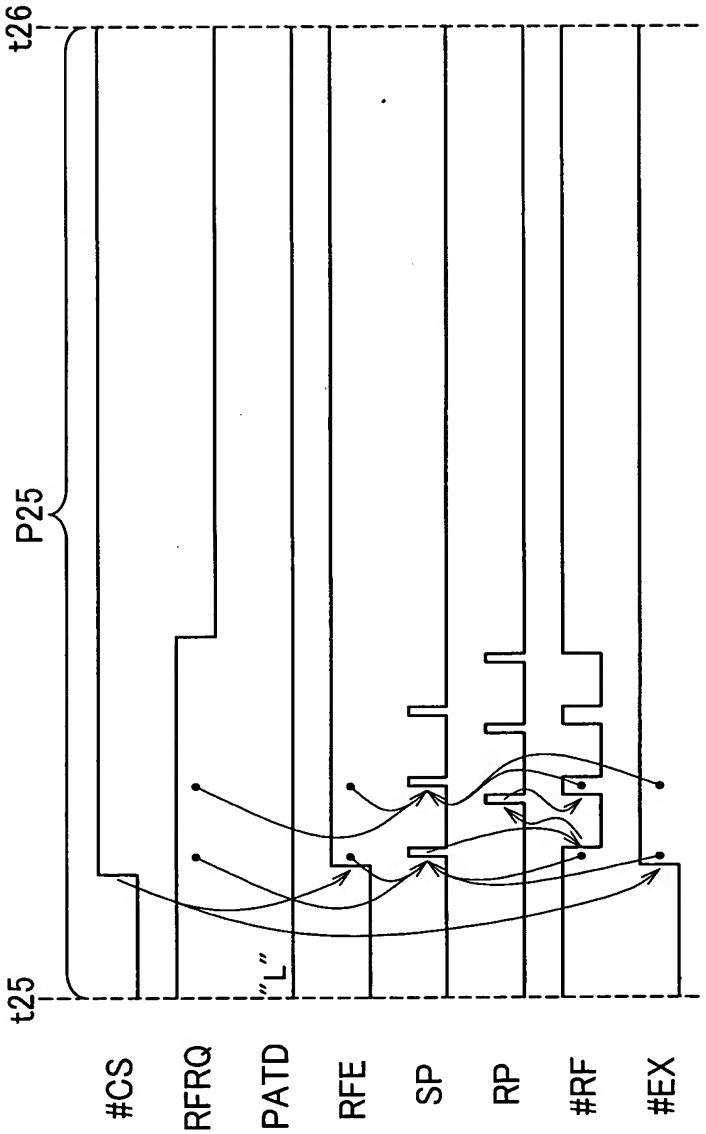


Fig.10

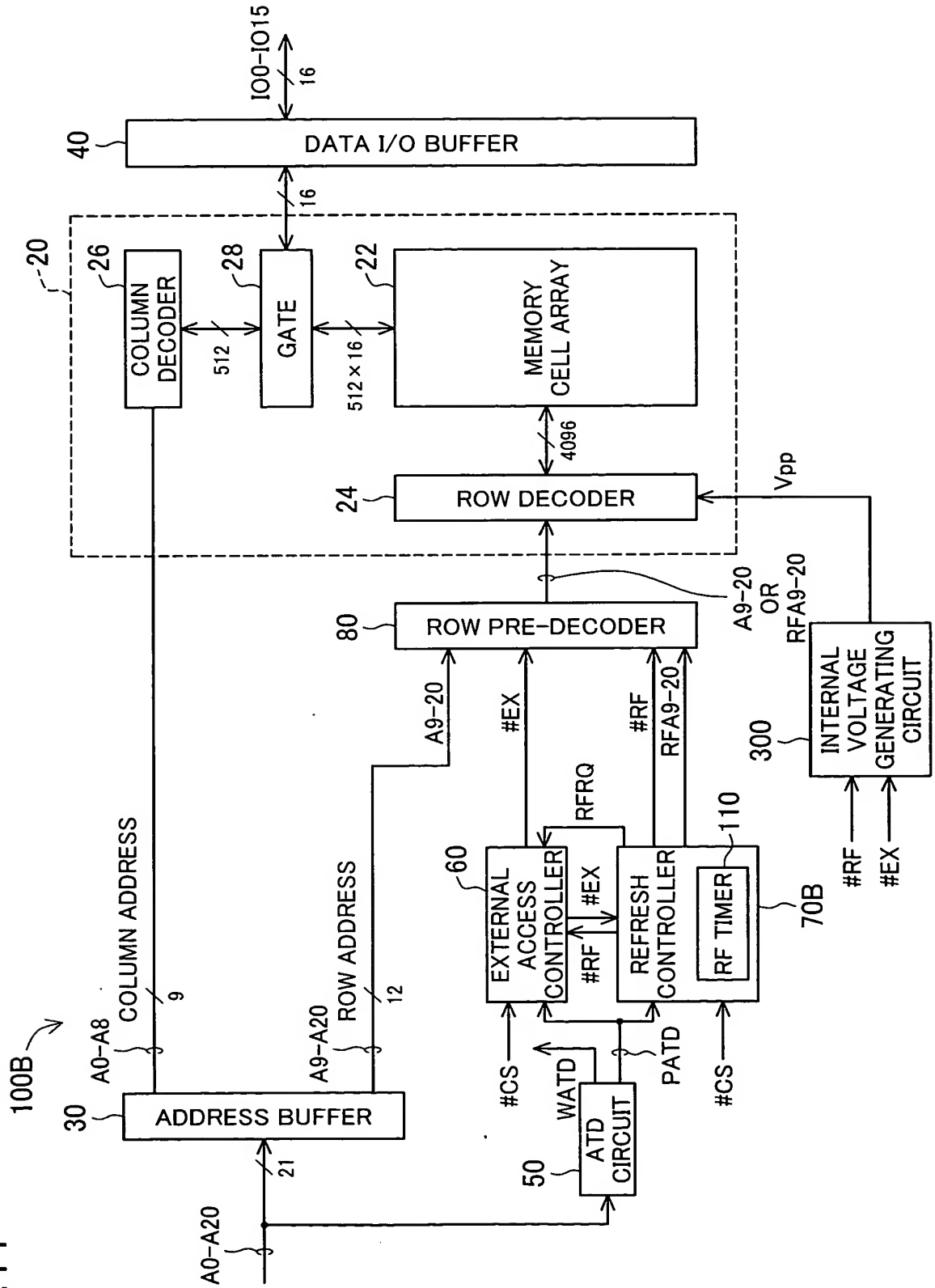

I00-I015
16
40
DATA I/O BUFFER
16
20
26
COLUMN DECODER
512
28
GATE
512×16
22
MEMORY CELL ARRAY
4096
24
ROW DECODER
Vpp
A9-20 OR RFA9-20
80
ROW PRE-DECODER
A9-20
#EX
#RF
RFA9-20
RFRQ
300
INTERNAL VOLTAGE GENERATING CIRCUIT
#RF
#EX
60
EXTERNAL ACCESS CONTROLLER
#EX
#RF
REFRESH CONTROLLER
110
RF TIMER
70B
COLUMN ADDRESS
9
ROW ADDRESS
12
100B
A0-A8
A9-A20
#CS
WATD
PATD
#CS
30
ADDRESS BUFFER
21
50
ATD CIRCUIT
A0-A20

Fig.11

Fig.12

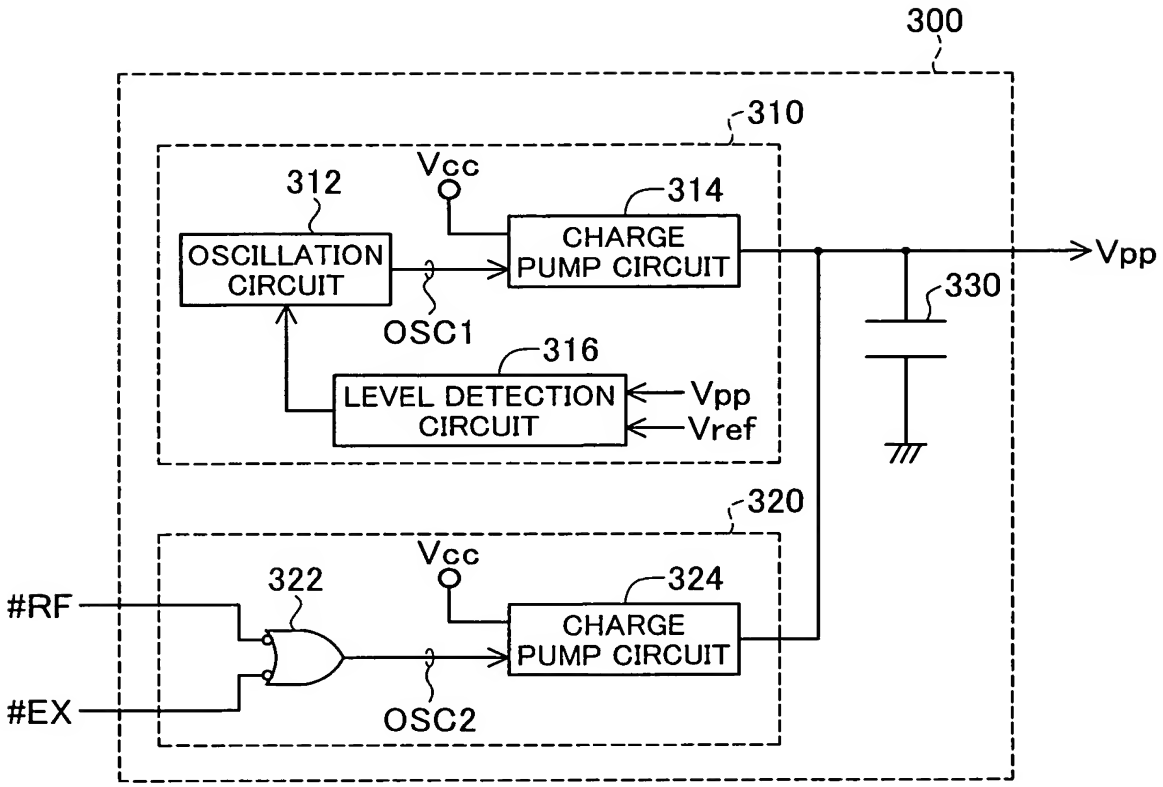

300
310
Vcc
312
314
OSCILLATION CIRCUIT
CHARGE PUMP CIRCUIT
Vpp
330
OSC1
316
LEVEL DETECTION CIRCUIT
Vpp
Vref
320
Vcc
322
324
#RF
CHARGE PUMP CIRCUIT
#EX
OSC2

Fig.13

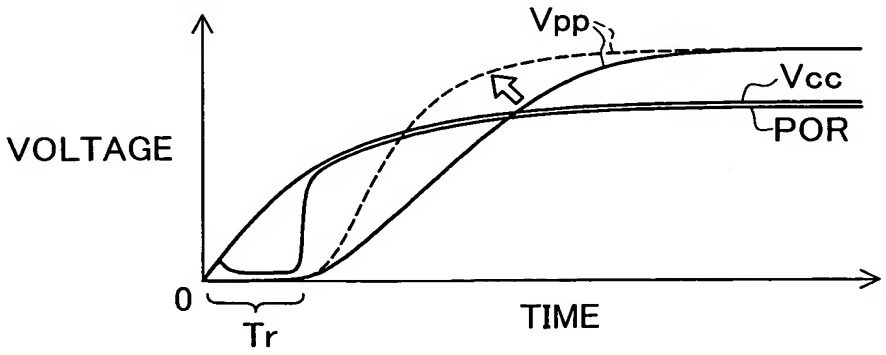

Vpp
Vcc
POR
VOLTAGE
0
Tr
TIME

Fig.14

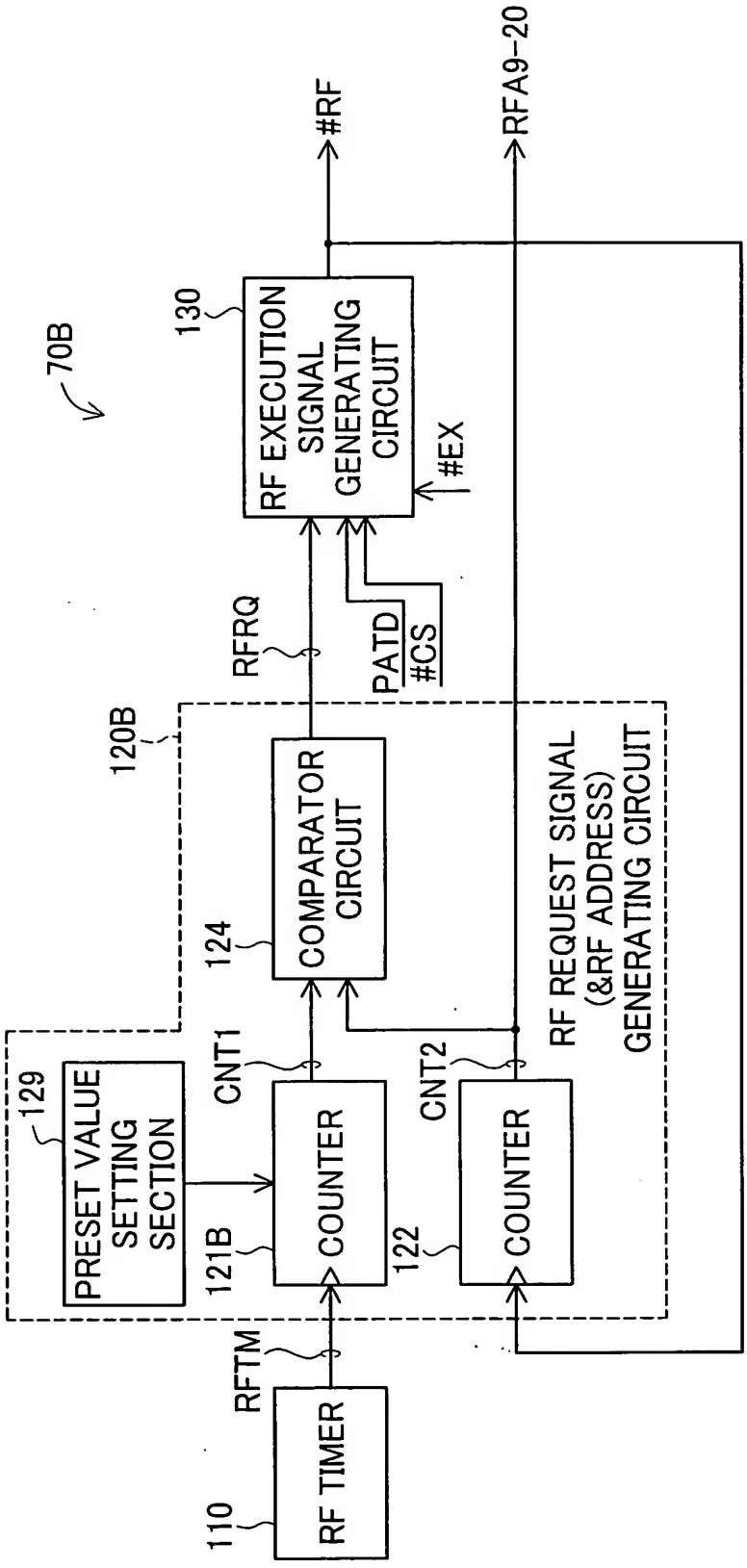

70B
110
RF TIMER
RFTM
120B
129
PRESET VALUE SETTING SECTION
121B
COUNTER
CNT1
122
COUNTER
CNT2
124
COMPARATOR CIRCUIT
RF REQUEST SIGNAL (&RF ADDRESS) GENERATING CIRCUIT
RFRQ
PATD
#CS
130
RF EXECUTION SIGNAL GENERATING CIRCUIT
#EX
#RF
RFA9-20

Fig.15(a) OSC2' (NO PRESET)

Fig.15(b) OSC2 (WITH PRESET)